WHAT IS CLAIMED IS:

1. A reading circuit for reading data from one memory cell of a plurality of memory cells, the reading circuit comprising:

a plurality of division sensing circuits each connected to the one memory cell via a sensing line corresponding thereto among a plurality of sensing lines; and

a current-voltage conversion circuit for converting a current flowing through each of the plurality of sensing lines into a sensing voltage representing a potential of each of the plurality of sensing lines,

wherein:

each of the plurality of division sensing circuits includes a current load circuit for supplying a current to the one memory cell via a corresponding sensing line among the plurality of sensing lines, and a sense amplifier for sensing a potential difference between the potential of the corresponding sensing line and a potential of a corresponding reference line of a plurality of reference lines, and

the current load circuit included in at least one division sensing circuit of the plurality of division

sensing circuits has a current supply capability which is different from the current supply capability of the current load circuit included in another division sensing circuits among the plurality of division sensing circuits.

2. A reading circuit according to claim 1, wherein the current-voltage conversion circuit includes a cell current division section for connecting or separating the plurality of sensing lines to or from the one memory cell.

3. A reading circuit according to claim 1, further comprising a first reference circuit for applying a first type of reference voltage representing a potential of one reference line among the plurality of reference lines to a sense amplifier corresponding to the one reference line among the plurality of sense amplifiers.

4. A reading circuit according to claim 1, wherein the current supply capability of each of the plurality of current load circuits is controlled by a first type of reference voltage representing a potential of a reference line corresponding thereto among the plurality of reference lines.

5. A reading circuit according to claim 1, wherein each of the plurality of current load circuits includes a PMOS transistor having a gate to which a reference voltage is to be applied via a reference line corresponding thereto among the plurality of reference lines.

6. A reading circuit according to claim 1, further comprising a second reference circuit for applying a second type of reference voltage for controlling the current supply capability of each of the plurality of current load circuits.

7. A reading circuit according to claim 6, wherein each of the plurality of current load circuits includes a PMOS transistor having a gate connected to the second reference circuit.

8. A reading circuit according to claim 1, further comprising:

a first reference circuit for applying a first type of reference voltage representing a potential of one reference line among the plurality of reference lines to a sense amplifier corresponding to the one reference line among the plurality of sense amplifiers; and

a second reference circuit for applying a second type of reference voltage for controlling the current supply capability of each of the plurality of current load circuits,

wherein the first reference circuit is electrically connected to the second reference circuit.

9. A reading circuit according to claim 2, wherein:

the cell current division section includes a plurality of NMOS transistors, and

each of the plurality of NMOS transistors includes a gate and a source connected to the gate.

10. A reading circuit according to claim 9, wherein:

each of the plurality of NMOS transistors is connected to a current load circuit corresponding thereto among the plurality of current load circuits, and

the current supply capability of each of the plurality of NMOS transistors is different in accordance with the current supply capability of the current load circuit connected to the corresponding NMOS transistor.

11. A reading circuit according to claim 10, wherein as the current supply capability of each of the plurality

of NMOS transistors is higher, the current supply capability of the current load circuit connected thereto is lower; and as the current supply capability of each of the plurality of NMOS transistors is lower, the current supply capability of the current load circuit connected thereto is higher.

12. A reading circuit according to claim 1, wherein the plurality of division sensing circuits operate in parallel.

13. A reading circuit according to claim 1, wherein each of the plurality of memory cells is a multi-level memory cell.

14. A reading circuit according to claim 3,

wherein the first reference circuit includes a plurality of reference voltage setting circuits, each of which includes:

a plurality of current load circuits each connected to a reference element via one sub reference line corresponding thereto among a plurality of sub reference lines, and

a current-voltage conversion circuit for

converting a current flowing through one sub reference line among the plurality of sub reference lines into a reference voltage representing a potential of the one sub reference line, and

wherein the reference voltage which is output from one reference voltage setting circuit among the plurality of reference voltage setting circuits controls the current supply capability of at least one of the plurality of current load circuits included in another reference voltage setting circuit among the plurality of reference voltage setting circuits.

15. A reading circuit according to claim 8,

wherein the second reference circuit includes a plurality of reference voltage setting circuits, each of which includes:

a plurality of current load circuits each connected to a reference element via one sub reference line corresponding thereto among a plurality of sub reference lines, and

a current-voltage conversion circuit for converting a current flowing through one sub reference line among the plurality of sub reference lines into a reference voltage representing a potential of the one sub

reference line, and

wherein the reference voltage which is output from the first reference circuit controls the current supply capability of at least one of the plurality of current load circuits included in one reference voltage setting circuit among the plurality of reference voltage setting circuits.

16. A reference circuit for generating a reference voltage for reading data from one memory cell among a plurality of memory cells, the reference circuit comprising:

a plurality of reference voltage setting circuits, each of which includes:

a plurality of current load circuits each connected to a reference element via one sub reference line corresponding thereto among a plurality of sub reference lines, and

a current-voltage conversion circuit for converting a current flowing through one sub reference line among the plurality of sub reference lines into a reference voltage representing a potential of the one sub reference line,

wherein the reference voltage which is output from one reference voltage setting circuit among the plurality

of reference voltage setting circuits controls the current supply capability of at least one of the plurality of current load circuits included in another reference voltage setting circuit among the plurality of reference voltage setting circuits.

17. A reference circuit according to claim 16, wherein each of the plurality of current-voltage conversion circuits includes a reference current division section for connecting or separating the plurality of sub reference lines to or from the reference element.

18. A reference circuit according to claim 17, wherein:

each of the plurality of reference current division sections includes a plurality of NMOS transistors, and

each of the plurality of NMOS transistors includes a gate and a source connected to the gate.

19. A reference circuit according to claim 18, wherein:

each of the plurality of NMOS transistors is connected to a current load circuit corresponding thereto among the plurality of current load circuits, and

the current supply capability of each of the plurality of NMOS transistors is different in accordance

with the current supply capability of the current load circuit connected to the corresponding NMOS transistor.

20. A reference circuit according to claim 19, wherein as the current supply capability of each of the plurality of NMOS transistors is higher, the current supply capability of the current load circuit connected thereto is lower; and as the current supply capability of each of the plurality of NMOS transistors is lower, the current supply capability of the current load circuit connected thereto is higher.

21. A reference circuit according to claim 16, wherein the reference element has substantially the same structure as that of each of the plurality of memory cells.

22. A reference circuit according to claim 16, wherein each of the plurality of current load circuits includes a PMOS transistor.

23. A reference circuit according to claim 22, wherein the PMOS transistor of one current load circuit among the plurality of current load circuits included in one reference voltage setting circuit among the plurality of

reference voltage setting circuits is current-mirror-connected with a PMOS transistor of one current load circuit among the plurality of current load circuits included in another reference voltage setting circuit among the plurality of reference voltage setting circuits.

24. A reference circuit for generating a reference voltage for reading data from one memory cell among a plurality of memory cells, the reference circuit comprising:

a first reference circuit; and

a second reference circuit,

wherein the first reference circuit includes a plurality of reference voltage setting circuits, each of which includes:

a plurality of current load circuits each connected to a reference element via one sub reference line corresponding thereto among a plurality of sub reference lines, and

a current-voltage conversion circuit for converting a current flowing through one sub reference line among the plurality of sub reference lines into a reference voltage representing a potential of the one sub reference line,

wherein the reference voltage which is output from one reference voltage setting circuit among the plurality of reference voltage setting circuits controls the current supply capability of at least one of the plurality of current load circuits included in another reference voltage setting circuit among the plurality of reference voltage setting circuits,

wherein the second reference circuit includes a plurality of reference voltage setting circuits, each of which includes:

a plurality of current load circuits each connected to a reference element via one sub reference line corresponding thereto among a plurality of sub reference lines, and

a current-voltage conversion circuit for converting a current flowing through one sub reference line among the plurality of sub reference lines into a reference voltage representing a potential of the one sub reference line, and

wherein the reference voltage which is output from the first reference circuit controls the current supply capability of at least one of the plurality of current load circuits included in a reference voltage setting circuit among the plurality of reference voltage setting

circuits of the second reference current.

25. A semiconductor memory device, comprising:

a memory cell array including a plurality of memory cells; and

a reading circuit for reading data from one memory cell among the plurality of memory cells,

wherein the reading circuit includes:

a plurality of division sensing circuits each connected to the one memory cell via a sensing line corresponding thereto among a plurality of sensing lines; and

a current-voltage conversion circuit for converting a current flowing through each of the plurality of sensing lines into a sensing voltage representing a potential of each of the plurality of sensing lines,

wherein each of the plurality of division sensing circuits includes a current load circuit for supplying a current to the one memory cell via a corresponding sensing line among the plurality of sensing lines, and a sense amplifier for sensing a potential difference between the potential of the corresponding sensing line and a potential of a reference line corresponding thereto among a plurality of reference lines, and

wherein the current load circuit included in at least one division sensing circuit among the plurality of division sensing circuits has a current supply capability which is different from the current supply capability of the current load circuit included in another division sensing circuits among the plurality of division sensing circuits.

26. A semiconductor memory device according to claim 25, wherein each of the plurality of memory cells is a multi-level memory cell.

27. A semiconductor memory device, comprising:

a memory cell array including a plurality of memory cells; and

a reference circuit for generating a reference voltage for reading data from one memory cell among the plurality of memory cells,

wherein the reference circuit includes a plurality of reference voltage setting circuits, each of which includes:

a plurality of current load circuits each connected to a reference element via one sub reference line corresponding thereto among a plurality of sub

reference lines, and

a current-voltage conversion circuit for converting a current flowing through one sub reference line among the plurality of sub reference lines into a reference voltage representing a potential of the one sub reference line, and

wherein the reference voltage which is output from one reference voltage setting circuit among the plurality of reference voltage setting circuits controls the current supply capability of at least one of the plurality of current load circuits included in another reference voltage setting circuit among the plurality of reference voltage setting circuits.